FPGA-Based Processor for High Frame-Rate Target Detection on Cluttered Backgrounds Using LVASI™ Sensors

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ABSTRACT

In our previous papers, the FPGA-based processing package and the co-processor board have been introduced for numerous commercial and military applications including motion detection, optical flow, background velocimetry, and target tracking. The processing package is being continually upgraded by new point- and area-applied algorithms for a variety of real-time digital video camera systems including foveal sensors based on Nova's **V**ariable **A**cuity **S**uperpixel **I**mager (VASI™) and **L**arge **F**ormat VASI™ (LVASI™) technologies.

This paper demonstrates the FPGA-based processor for high frame-rate target detection in a cluttered background using variable acuity sensors. For the 1024 x 1024 pixel LVASI™ Focal Plane Array (FPA), the proposed target-detection algorithm increases the frame rate from 4 Hz for the full resolution mode up to 450 Hz for the foveal mode while maintaining full field of view and target-detection performances on cluttered backgrounds that are comparable with detection performances at the full resolution mode.

Keywords: Foveal Sensors, Image Processor, FPGA, FPA, Variable Acuity, Superpixels, Programmable, Visible, Infrared, UAV, Target Detection, Cluttered Background Rejection

1. INTRODUCTION

Nova Sensors has developed a new class of imaging sensors, "foveal sensors" using principles of functioning of human vision. In contrast to full-resolution sensors, foveal sensors provide a wide field of view at high frame rates with one or more very high spatial resolution regions (i.e., foveae) on areas of interest. The foveal sensors are based on Nova's VASI™ [1] and LVASI™ (frame size of 1024 x 1024 pixels) technologies [2], [3].

The foveal VASI™/LVASI™ sensors provide the capability for the user or controlling processor [5] to change the spatial configuration of high- and lower- spatial resolution pixels *at the frame rate*. Spatial configuration of pixels in the imager may be realized by programming the device to permit pixels to share their individually-collected photocharge with any or all of their neighbors. The multi-resolution characteristics of such sensors help to reduce the total number of effective pixel values that are multiplexed off of the focal plane array (FPA) with each frame, thereby reducing the data bandwidth required to produce an accurate representation of the salient portions of the image, while continuing to observe the total field of view (TFOV) at lower resolutions.

It is evident that the FPGA-based controlling processor and the algorithm-package designed at Nova Sensors are important components of VASI™ sensors. In our previous papers, the FPGA-based processing package [4] and the co-processor board [5] have been introduced for numerous commercial and military applications including motion detection, optical flow, background velocimetry, and target tracking. The processing package [4] is being continually upgraded by new point- and area-applied algorithms [6]-[9] for variety of real-time digital video camera systems including foveal sensors [1] - [3].

The goal of this paper is to demonstrate the FPGA-based processing package for the high frame-rate target detection on a cluttered background using variable acuity sensors (see Section 3).

This paper is organized as follows. Section 2 contains an overview of VASI™ and LVASI™ sensors as well as a brief description of the image processor and the FPGA-based algorithm package. Section 3 demonstrates techniques for the high frame-rate target detection on cluttered backgrounds using LVASI™ sensors. Section 4 introduces Method-3 for the FPA read-out format to increase the overall frame-rate of foveal sensors.

2. OVERVIEW OF VASI™ SENSORS FOR REDUCING BANDWIDTH AND INCREASING FRAME-RATE OF IMAGE DATA WHILE MAINTAINING FULL FIELD OF VIEW & FULL RESOLUTION IN AREAS OF INTEREST

2.1. VASI™ Sensors Concept

Nova Sensors has developed a novel two-dimensional imaging chip [1] - [3] whose design is based on properties exhibited by biological retinas. The VASI™ imager permits the user to program a unique spatial arrangement of "superpixels" that may be updated in real time and at the operational frame rate.

Any spatial configuration of pixels in the imager may be realized by programming the FPA to permit pixels to share their individually-collected photocharge with any or all of their neighbors. Two bit maps (called "Left"- and "Up", discussed in Section 2.2) are used to program the FPA. Single and multiple "foveal" configurations are possible, and these high spatial resolution regions may be "flown" around the FPA controlled by an embedded FPGA based processor.

Figure 1 illustrates the major VASI™ concept of replacing a full-resolution a)-image by a foveae d)-image to "compress" the image data flow. Image "compression" means the reduction of the total number of effective pixel values that are multiplexed off of the focal plane array (FPA).

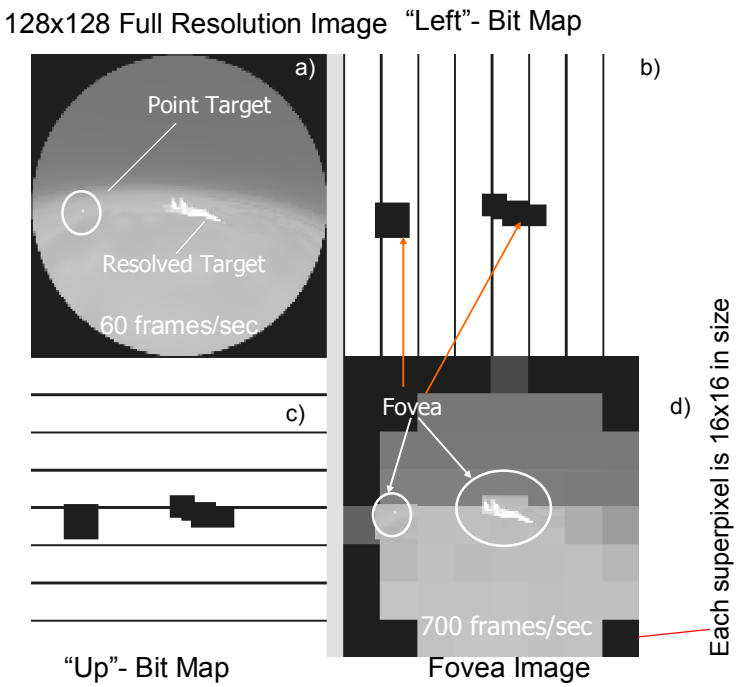

Figure 1. VASI™ Sensors Concept: Replacing of a full-resolution a)-image by a foveae d)-image to compress the image data flow.

The full resolution a)-image was generated by the CHAMP infrared scene generation program [10], [11]. Both a) and d) images (see Figure 1.a and Figure 1.d) contain a point-target and a resolved target image. The size of the full resolution frame a) is 128x128 pixels. The superpixel size in the superpixullated image d) is 16x16 pixels. This superpixel configuration with two foveal regions d) produces 23 times less pixel values per frame than the full resolution image a).
The b) and c) images represent the "Left" and "Up" bits, respectively, used to program the configuration shown in the image d). In the b) and c) images, the black rectangles correspond to zeroed bit of the "Left"- and "Up"-maps indicating the foveae location in image d).
Figure 1 demonstrates that VASI™ technology reduces the image data from 16384 pixel values (for the full resolution a)-image) to 718 pixel values (the "compressed" superpixelated d)-image).

2.2. FPA Read-Out Formats: "Up"-bit and "Left"-bit Controller

To change the spatial configuration of high- and lower spatial resolution pixels at the frame rate, the VASI™ Pre-Processor firmware design performs the following functions on the sensor data stream:
- "Up"-bit and "Left"-bit Controller to program the VASI™ FPA,
- Image Reconstruction from the "compressed" format to the full-resolution format (see Figure 1),
- Bad Pixel Replacement (BPR), and
- Non-Uniformity Correction (NUC).

"Up" and "Left" denote the connectivity between an individual pixel and its upward and leftward nearest neighbors. Each pixel is programmed into a specific "superpixel" state, and it will "know" how to share its charge with neighbors so that a resulting superpixel distribution is produced.

Two different implementations have been developed to control the spatial configuration of pixels in Nova Sensors' variable spatial acuity products.

2.2.1. "Up"-bit and "Left"-bit Controller for VASI™

The first technique [3] makes use of two bits of SRAM that reside in each pixel of the 320 x 256 imager format; these bits control the connection of the pixel's integration capacitor to the "Up" and the "Left" neighboring pixels, respectively (see Figure 2).

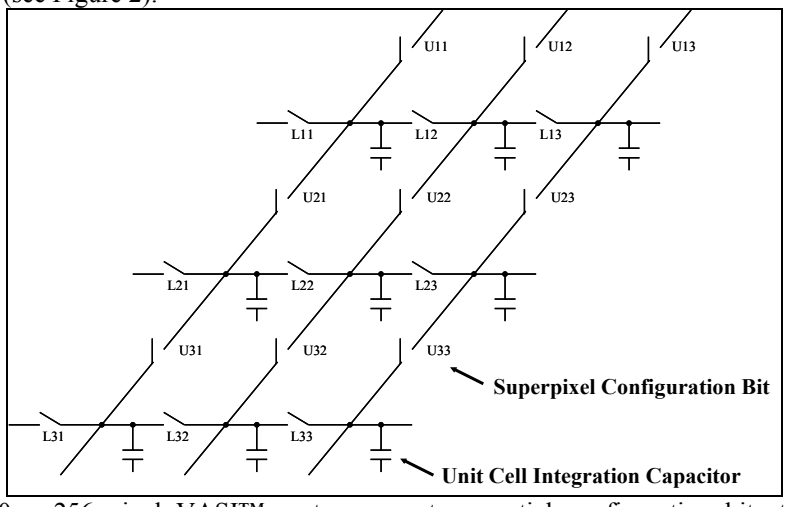

Figure 2. The 320 x 256 pixel VASI™ system uses two spatial configuration bits to control "in cell" connections, resulting in local spatial averaging control.

The two-bit spatial configuration codes must be programmed into the imaging array in such a way that the on-chip spatial averaging functionality may be realized. A great advantage of this technique is that since each "superpixel" need only be read out one time (instead of reading out all "native" pixel values that produce the superpixel's on-chip average), the readout time is much shorter than for a conventional imaging device.

Figure 3 shows the example of programming codes that would be required to produce the spatial configuration for a central "fovea" region with 4 x 4 superpixel average regions. Again, the bit pair indicates the (up, left) connections where "1" indicates a closed switch.

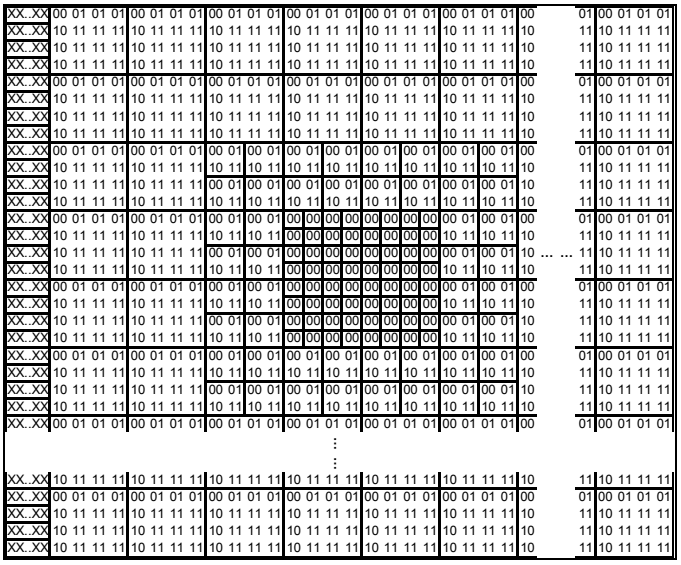

Figure 3. The two-bit programming codes shown create a central foveal region.

2.2.2. "Up"-bit and "Left"-bit Controller for LVASI™

Nova's newest device, a 1024 x 1024 (i.e., "1K x 1K") pixel infrared Large Format VASI™ imager LVASI™, requires the unit cell (19.5 um pitch) to be smaller than that of the 320 x 256 device (30 um pitch) due to reticle size limitations of the overall die. Because of this, Nova had to reduce the number of in-cell spatial configuration bits from two to one [3], [10].

LVASI™ FPA: Method-1

Two read-out methods were proposed to control the superpixel in the large format LVASI™ FPA: Method-1 and Method-2 (see Figure 4 and Figure 5, correspondingly).

The major characteristics of foveal control in Method 1 are:

- SRAM bit in each unit cell enables charge sharing into U, L superpixel lattice
- U, L and SRAM bit decoded by X/Y shift-registers for column/row readout
- Multiple foveae of any shape allowed

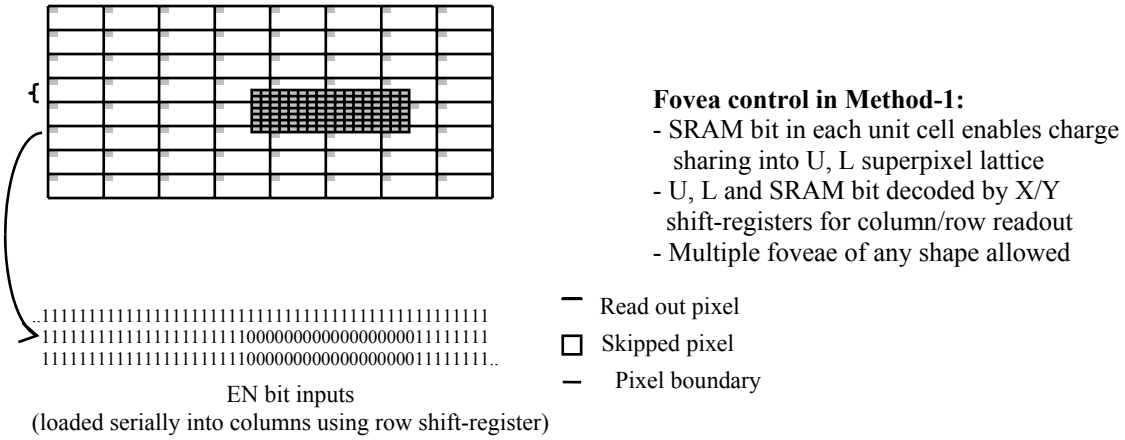

Figure 4. LVASI™ Method-1 read-out format.

LVASI™ FPA: Method-2

In LVASI™-M2, the 1K x 1K uses two one-dimensional registers to control the superpixel configuration, as shown in Figure 5. This particular image shows how the use of the two one-dimensional "U" and "L" superpixel configuration registers may also be used to produce regions of highest spatial resolution referred to as "pseudo-foveae". The spatial configuration of the imaging device may be changed at the frame rate. This particular technique allows the highest possible frame rates that permit foveae to be "flown" around the image at the will of the controlling processor. In certain spatial configuration modes, this "Large VASI™" device (LVASI™) has the capability of imaging the entire 1K x 1K field of view at frame rates in excess of 1000 frames/second (see example in Section 3)

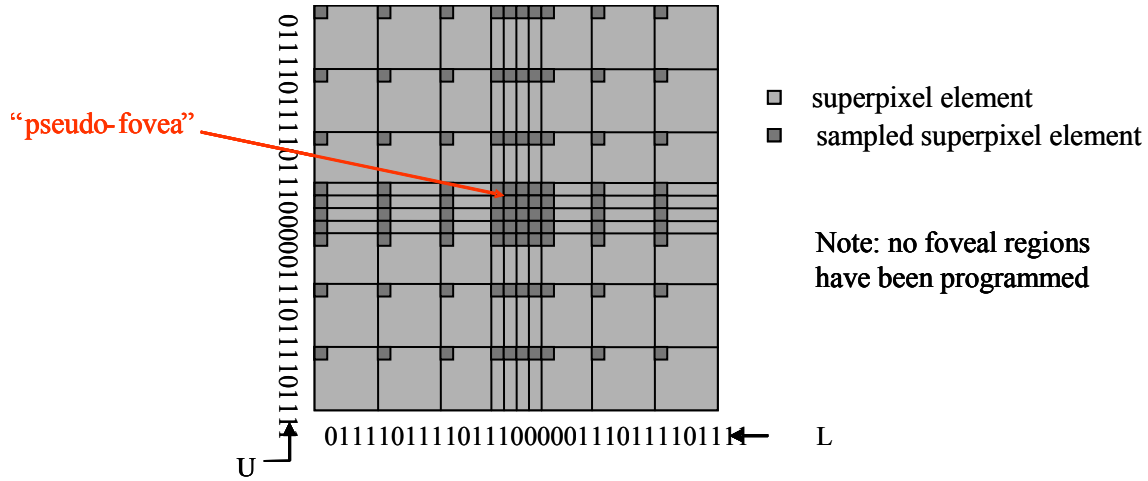

Figure 5. LVASI™ Method-2 read-out format: Nova's 1K x 1K LVASI™-M2 device uses two 1-dimensional registers to set the superpixel configuration, and a single "in-cell" bit to isolate a pixel from its neighbors, causing it to be a "foveal pixel". This U/L-map format (LVASI™ Method-2 read-out format) allows for increasing of the frame rate (see Figure 12 and Figure 13).

High frame rates are possible using VASI™/LVASI™ technology by programming the device into a superpixel state; pixels (whether "standard pixels" or "superpixels") need to deliver only one analog data value per frame. This will minimize the total number of pixel values to be read off of the FPA ("compressed" images are read off FPA), thus maximizing the effective frame rate. An example of "Left"- and "Up"- maps is presented in Figure 1 (see images b) and c), respectively). These maps have been used, correspondingly, to program the configuration shown in the image d. Four dark areas/rectangular in Figure 1 (images b and c) correspond to the four foveae. Their coordinates and dimensions have been computed by the Multiple Target Acquisition function of the master image-processing card (see Figure 6 and Figure 7). In the given example (Figure 1) the image size is 128x128 pixels, the superpixel size is 16x16 pixels, and the image data have been reduced by VASI™ technology from 16384 pixel values (full resolution image) to 718 pixel values (see the "compressed" superpixelated image on the right figure of Figure 1). The detailed analysis of frame-rate increase using for LVASI™ Method-1 and Method-2 are given in Section 3.

2.3. Image Processor Board and Algorithm Package

Designed according to principles of human vision, VASI™ sensors will enable a large new class of real-time algorithms specifically designed for autonomous target acquisition (ATA) and tracking targets of interest. To date, Nova Sensors has produced a variety of "first-cut" acquisition algorithms for the VASI™. These algorithms (see Table 1) are being implemented into Nova Sensors' miniature image processor board that was introduced in [5] (see Figure 6 and Figure 7).

Table 1. Point- and area-applied algorithms included in the advanced image-processing package.

Point-applied algorithms implemented in FPGA:	Area-applied algorithms implemented in FPGA:
- Image reconstruction from a compressed frame - One- and two-point non-uniformity correction including the median offset computation from the masked FPA-row data - Arbitrary pixel revectoring - Bad pixel replacement - Pixel-based mean and standard deviation computation - Spectral attenuation compensation - Atmospheric attenuation compensation	- Intensity-weighted centroid target tracking (up to four targets) - Real-time Fast Fourier Transform (FFT) and Power Spectral Density (PSD) computation - Convolution processing - Median and average filters - Optical flow vector field computation - Background velocimetry - Zero Crossing Technique (ZCT) - Morphologically-based Target Acquisition

The detailed analysis of the image-processing technique listed in Table 1 have been provided in our previous paper [4]. The processing package is being continually upgraded by new point- and area-applied algorithms [6]-[9].

Figure 6 shows a photograph of the miniature image processor board set. The board set includes a number of Xilinx Virtex II FPGA devices (each part contains at least one million gates of programmable logic) to support a wide variety of processing algorithm operations and incorporates enough static RAM to support growth to image sizes of up to 2048 x 2048 pixels per frame. The processor board set is capable of receiving digital camera image data at effective total pixel rates of up to 80 megapixels/second. Depending upon the complexity of the processing function, multiple boards can be interfaced to partition the task into multiple parallel processing streams. More details regarding processor board performance have been presented in [5].

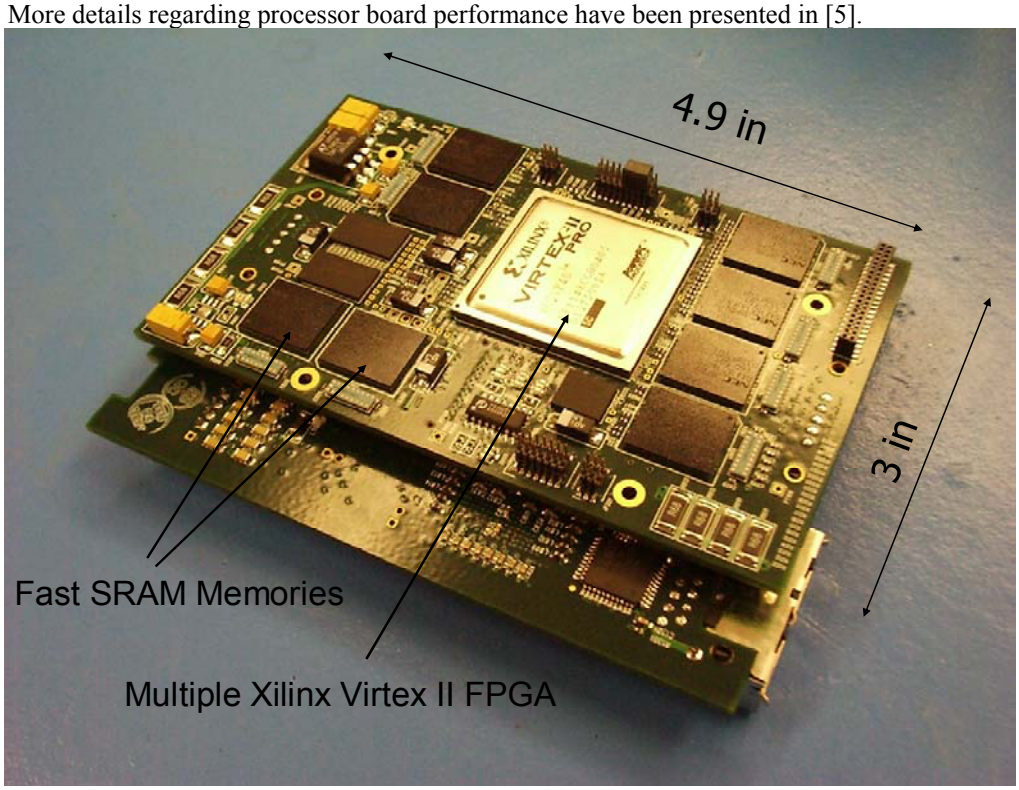

Figure 6. Nova's miniature image/signal processor board set, designed to incorporate multiple Xilinx Virtex II FPGAs and fast SRAM memories.

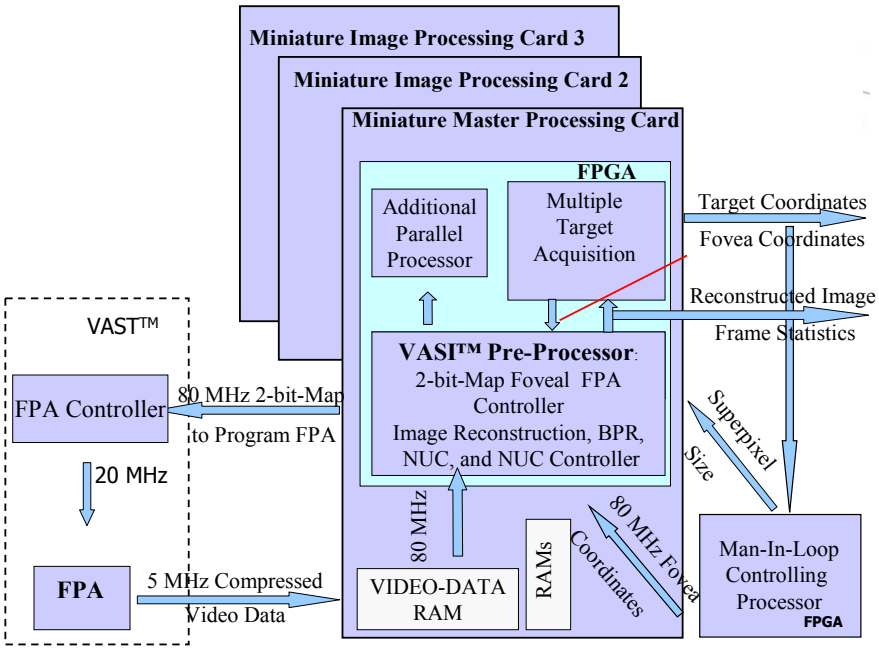

Figure 7. Fully Re-programmable Miniature Image Processor Board for VASI™ Sensors.

2.4. VASI™ Sensors for Reducing Bandwidth and Increasing Frame-Rate of Image Data

Figure 8 - Figure 9 illustrates the major advanced features of VASI™ sensors valuable for target acquisition and tracking system. Allocation of the full resolution 32 x 32 fovea at the area of interest while maintaining 16 x 16 superpixels in a 320 x 256-pixel frame allows for increasing of frame rate from around 40Hz (for the full-resolution frame) up to 530 Hz (for the foveated frame) with simultaneous decreasing of bandwidth from 33 MBps to 13 MBps, correspondingly (see Figure 9).

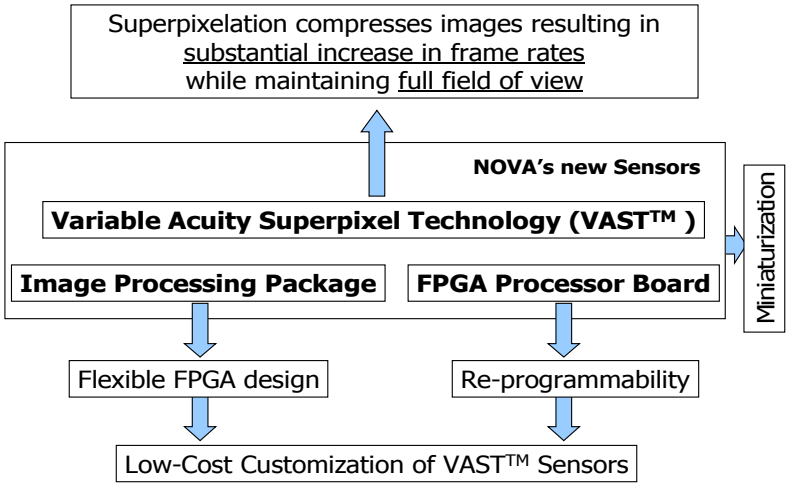

Figure 8. Major Advanced Features of VASI™ Sensors.

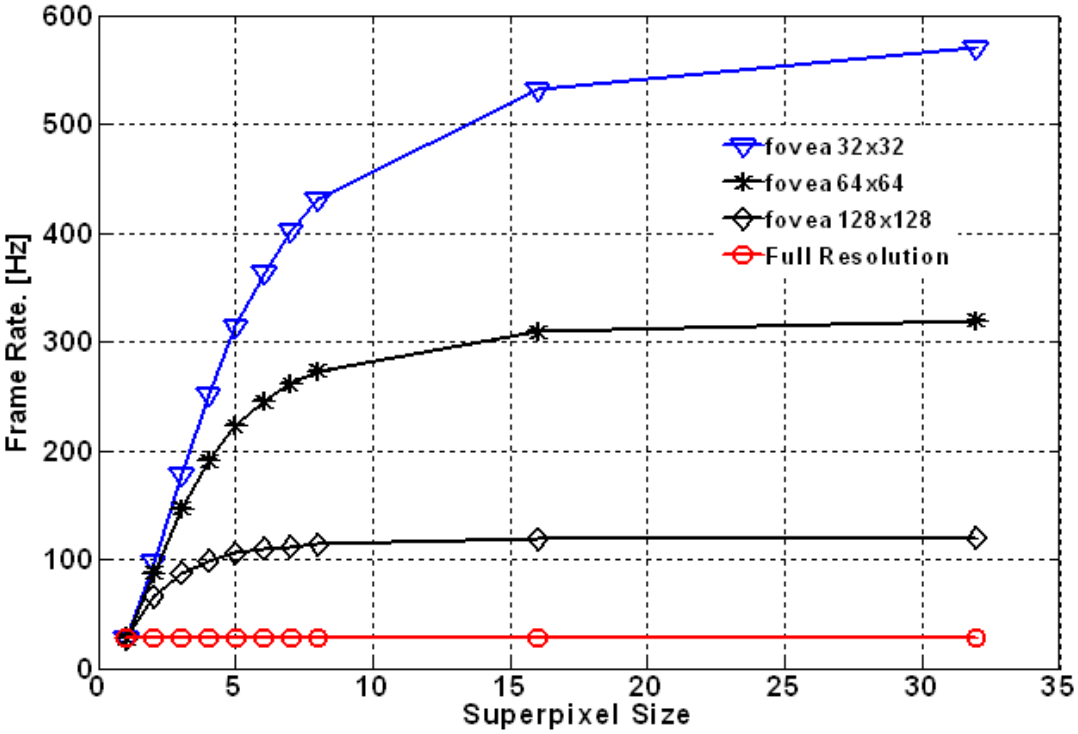

Figure 9. VASI™ FPA frame rate as a function of superpixel size. Allocation of the full-resolution 32x32 fovea at the area of interest while maintaining 16x16 superpixels in 320x256-pixel frame allows for increasing of frame rate from around 40 Hz (for the full resolution frame) up to 530 Hz (for the foveated frame) while simultaneous decreasing the bandwidth from 33 MBps to 13 MBps, correspondingly.

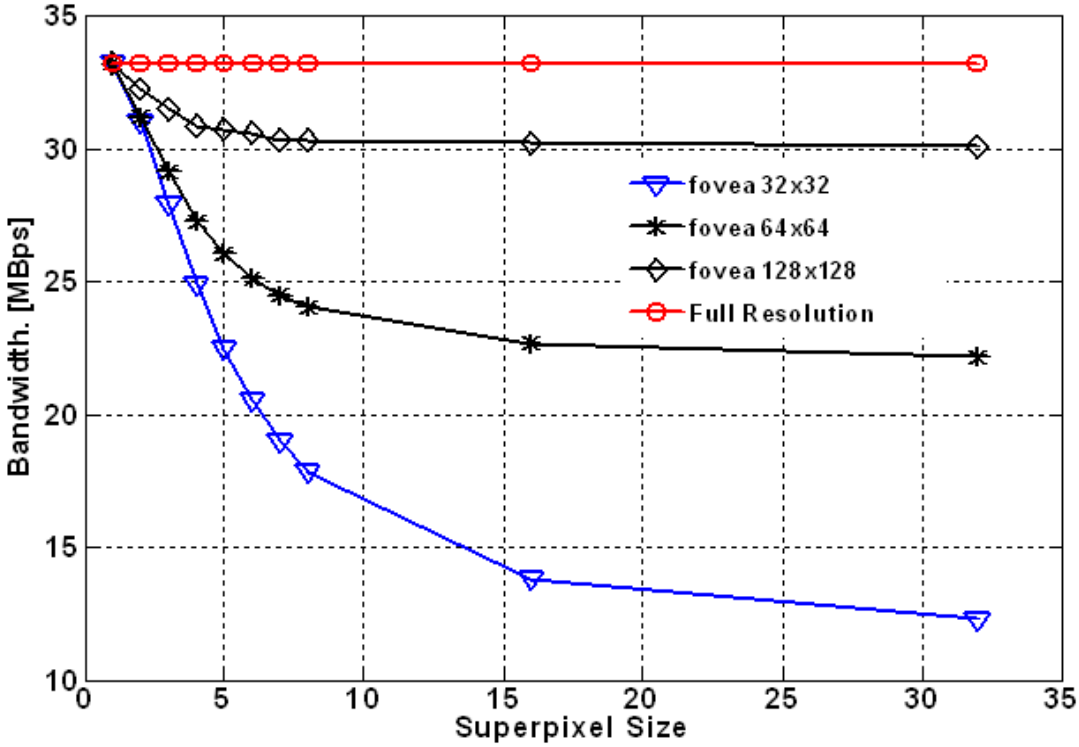

Figure 10. VASI™ FPA bandwidth as a function of superpixel size

3. HIGH FRAME-RATE TARGET DETECTION ON CLUTTERED BACKGROUNDS USING LVASI™ SENSORS

Under the AFA (Acquisition and Tracking Algorithms to Exploit Foveal Sensors, Contract FA8651-05-C-0240) Phase-1 project, Nova Sensors has demonstrated the concept of the high frame-rate target detection on cluttered backgrounds using LVASI™ sensors. To achieve the best target-detection performances on cluttered background using the 1024x1024 pixel focal plane array (FPA), the sensor operates at full-resolution mode at 4 frame-per-second until target detection. Once a target is detected, the sensor detects the target in the foveae mode at the highest frame-rate of 450 Hz (see Figure 11).
To suppress false alarms from cluttered background, the four-target tracker involves a morphological filter [4], [12] with adaptive threshold computation using Renyi's entropy [13],[14], as well as the optical flow algorithm [15], [16] computing velocities for the background and for each candidate to target. Figure 11 illustrates false alarm suppression as well as target detection at 450 frame-rate. The left image in Figure 11 is the superpixelated frame with a fovea around the detected target. The middle image is the cumulative history of targets and false alarms detected before optical flow is considered and used to compensate for apparent background motion. The right image is the target trajectory detected after incorporation of optical flow. False alarms are suppressed effectively while the frame rate is increased from 4 Hz in full resolution mode to 450 Hz in foveated mode.

Figure 12 illustrates the FPA frame rate as a function of fovea size for VASI™, LVASI™-M1 and LVASI™-M2 techniques. The read-out formats of these methods are presented in Section 2. For the Large Format VASI™ of 1024x1024 pixels and FPA programming method 2 (see LVASI™-M2 curves), the frame rate is 450 Hz at a superpixel size of 16x16 and fovea size of 32x32.

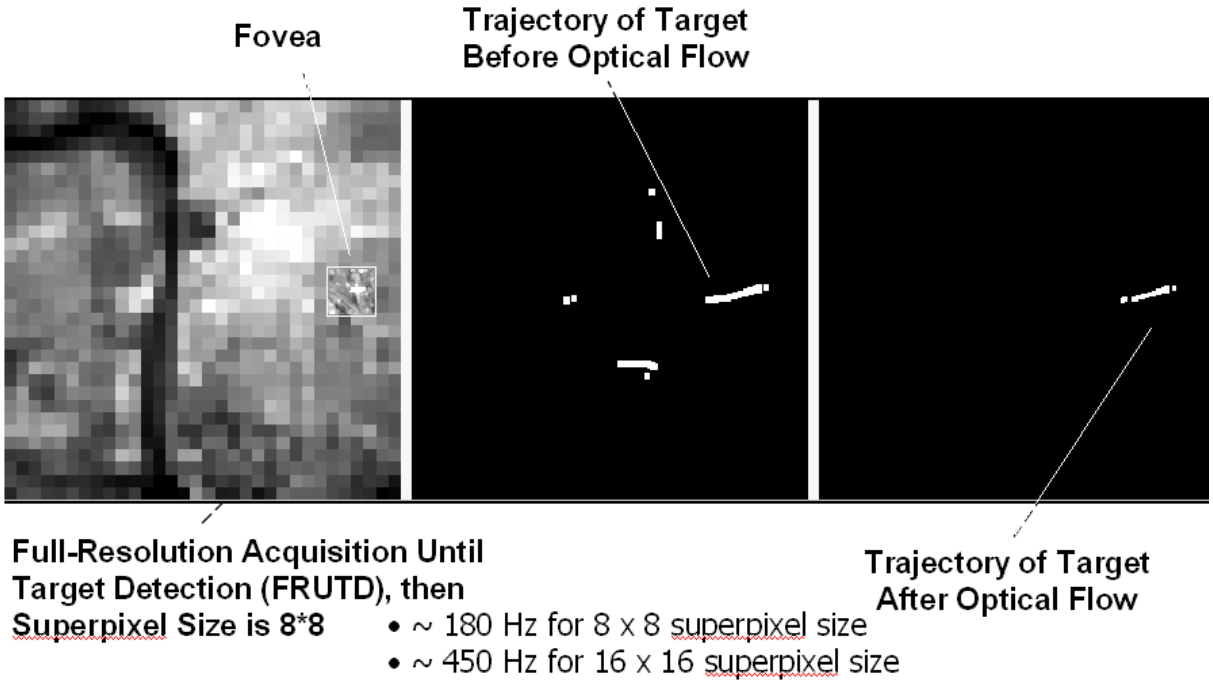

Figure 11. The left image is the superpixelated frame with a fovea around the detected target. The middle image is the cumulative history of targets and false alarms detected before optical flow is considered and used to compensate for apparent background motion. The right image is the target trajectory detected after incorporation of optical flow. False alarms are suppressed effectively while the frame rate is increased from 4 Hz in full resolution mode to 450 Hz in foveated mode with the superpixel size of 16x16 pixels.

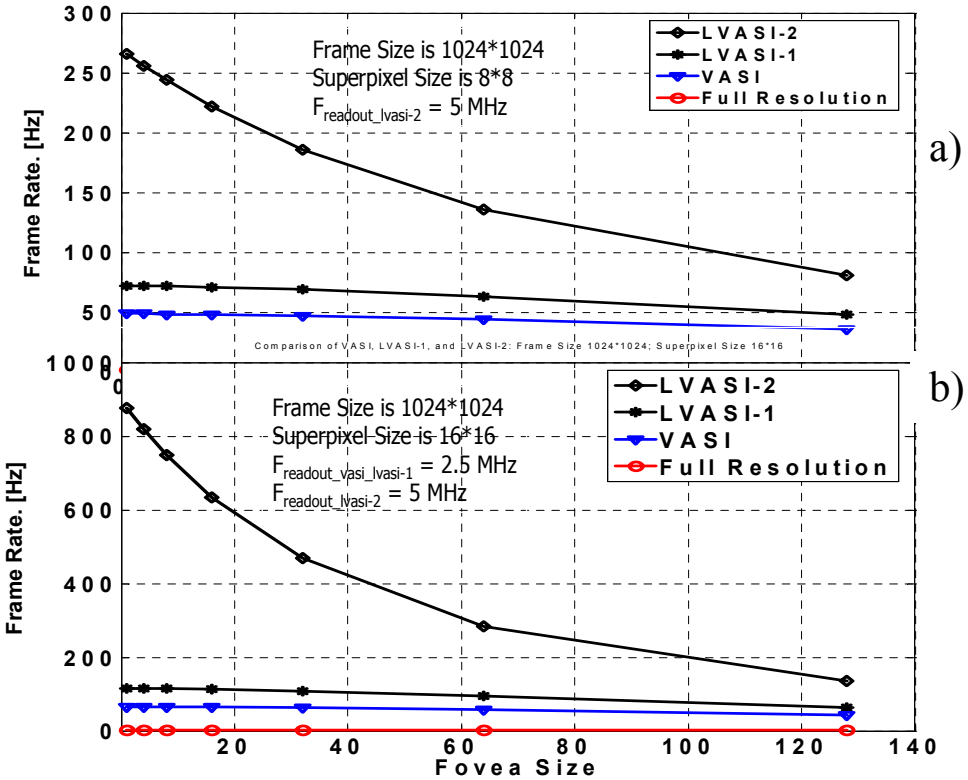

Figure 12. FPA frame-rate as a function of fovea size: comparison of VASI™ and LVASI™-M1, and LVASI™-M2 techniques. a) – superpixel size is 8x8 pixels; b) – superpixel size 16x16 pixels.

4. LVASI™ METHOD-3: INCREASING OF PROCESSING FRAME-RATE FOR THE 1K*1K-SENSOR FROM 76 HZ UP TO A FEW HUNDREDS FRAMES PER SECOND

The previous Section 3 shows the advantage of using LVASI™-M2 technology for increasing of the FPA frame-rate. In spite of the high read-out frame-rate of an LVASI™ 1K*1K Focal Plane Array (see Figure 12 and Figure 13, curves LVASI™-M2), the overall frame-rate for LVASI™ sensors is limited by the 76 frame-per-second limit of the 1Kx1K FPGA processor running at 76 MHz (see Figure 13, curve "M1 & M2 Image Processor Limit"). To overcome the above mentioned 76 frame-per-second limitation, the LVASI™-Method-3 has been proposed to create the multiple read-out-FPA channels delivering the compressed video data. These multiple read-out channels are the virtual ones.

The idea of the FPA read-out Method-3 is that Method-2 is used sequentially a few times in order to create a few sequential (for a given frame) read-out channels: the first channel is the compressed superpixelated frame (no foveae); the other channels (the 2nd, 3rd, 4th and the 5th channels) contain the FPA readings from the corresponding fovea areas only. These five heavily compressed data streams allow re-using the same image processing package for tracking targets (up to four targets) in the superpixelated/compressed frame and in each fovea separately, at extremely high frame rate, while reconstructing these five data streams to the full 1Kx1K image at slow rate for display/visualization only.
Figure 13 illustrates that, because of the 76MHz frequency-limit of the Image Processor board, an LVASI™-M2 1Kx1K sensor cannot be operated faster than 76 frame-per-second (no matter which method is used, i.e., Method-1 or Method-2). In other words, curves LVASI™-M1 and LVASI™-M2 have to coincide with the "M1 & M2 Image Processor Limit" curve of 76 Hz.

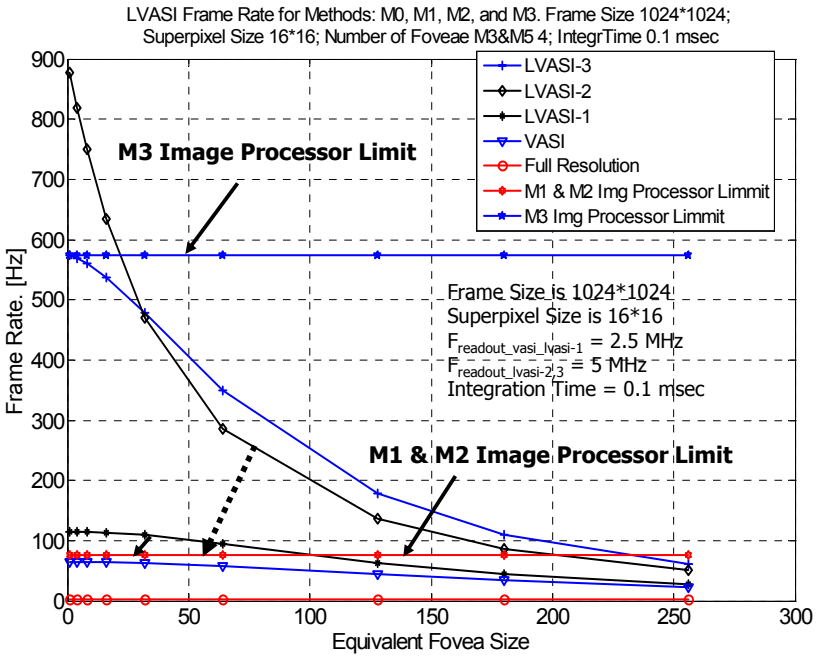

Figure 13. Demonstrates sufficient increase of the sensor frame-rate for the proposed LVASI™ Method-3 up to a few hundred frames-per-second. All curves except the LVASI™-M3 curve are for one fovea. The curve LVASI™-M3 is plotted for four foveae. The equivalent fovea-size is the size of a fovea in Method-1/Method-2 that is equal in area to the total area of four foveae in Method 3. The curves LVASI™-M1 and LVASI™-M2 have to coincide with the "M1 & M2 Image Processor Limit" curve of 76 Hz. The frame size is 1Kx1K pixels. The superpixel size is 16x16 pixels. The integration time to read the video data for each channel is 0.1 msec. The actual frequency of the M-3 Image Processor is higher than 1147 Hz: the corresponding "M3 Image Processor" curve lowered to the maximum frame rate of Method-3 to fit the Figure 13.

In contrast to Method-1 and Method-2, the proposed FPA read-out Method-3 (see LVASI™-M3 curve in Figure 13) is not limited by the M-3 Image Processor (see the "M3 Image Processor" curve). The actual frame-rate of the M-3 Image Processor is higher than 1147 Hz, and the corresponding "M3 Image Processor" curve in Figure 13 is lowered to the maximum frame rate of Method-3 to fit the Figure 13.

To conclude, the proposed FPA read-out Method-3 allows for increase of the overall sensor frame-rate from 76 Hz (76 Hz is the limitation of the 1Kx1K Image Processor board running at 80 MHz clock), to a few hundred frames-per-sec (up to 500 Hz) while superpixel size is 16x16, the frame size is 1Kx1K, and integration time is 0.1 msec.

5. CONCLUSIONS

For the Large Format of 1Kx1K-pixels Variable Acuity Imager (LVASI™) developed by Nova Sensors, the M3 readout-from-FPA technique and the target-detection algorithm have been proposed to increase the processing frame-rate from 4 Hz for the full resolution mode up to 450 Hz for the foveal mode while maintaining full field of view and target-detection performances on cluttered backgrounds that are comparable with detection performances at the full resolution mode (see Sections 3 and 4).
An effective application of LVASI™ for the high frame-rate target detection using LVASI™ sensors is demonstrated (see Figure 11).

The VASI™ and LVASI™ concept (Section 2) as well as the major performances of FPGA-based processing board (see Figure 6) and image-processing algorithms (see Table 1) implemented in FPGA are discussed in the paper. Flexible FPGA designs of these techniques and re-programmability of the processing board allows for

low-cost and quick turn-around of customized applications of VASI™ and other state of the art imaging sensors, taking into account specific customer requirements. The processing package is being continually upgraded by new point- and area-applied algorithms [6]-[9].

6. ACKNOWLEDGEMENTS

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